UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,225	06/09/2000	David Robert Baldwin	TD-155	3467

29106 7590 11/30/2004

GROOVER & HOLMES
BOX 802889
DALLAS, TX 75380-2889

EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,225	BALDWIN, DAVID ROBERT	
	Examiner	Art Unit	
	Kee M Tung	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,15,17 and 20* is/are allowed.

6)☒ Claim(s) *1-5,7-13,16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 8/19/04 has been considered in preparing this Office action.

Claim Rejections - 35 USC § 112

2. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claimed "CPU **includes** a user input device, a microprocessor, and a data output device" is not described nor shown in the drawings.

3. Claims 2 and 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 2, line 3, the phrase "... from dedicated graphics memory into a main memory" is indefinite because it is unclear how the "graphics accelerator unit manages page faulting of texture data from dedicated graphics memory into a main memory" as claimed. Clarification or correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 3 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Mizuyabu et al (6,297,832 hereinafter "Mizuyabu").

As per claim 1, Mizuyabu teaches a computer system (Fig.1 shows a video graphics system which is a part of the computer system) comprising a graphics accelerator unit (Fig. 1, video graphics system) which manages page faulting (memory controller 20 manages page faults, col. 5, lines 1-3) of texture data (shows texture data also stored in the memory 10, col. 4, lines 55-58) invisibly to the host processor (Fig. 1 shows the memory controller 20 coupled between memory 10 and a plurality of memory clients and does not involved host processor and thus is considered invisible to the host processor).

As per claim 3, Mizuyabu teaches a computer system (Fig.1 shows a video graphics system which is a part of the computer system) comprising at least one CPU (not shown in Fig. 1, but is inherent to any well known computer system to include at least one CPU), operatively connected to have read/write access to a main memory

(also not shown in Fig. 1 but is also inherent to any well known computer system to include a main memory); first memory management logic (also not shown in Fig. 1, but is also inherent to any well known computer system to include MMU to manage virtual memory), which virtualizes said main memory with reference to at least one bulk storage unit (such, as, disk memory, by definition from Microsoft Press Computer Dictionary, virtual memory may be partially simulated by secondary storage such as a hard disk); a graphics accelerator unit (Fig. 1, video graphics system), comprising rendering accelerator logic (Fig. 1, 3D/2D graphics image processor 70 and 80), dedicated graphics memory (memory 10), and a second memory management unit (memory controller 20) which manages texture data (shows texture data also stored in the memory 10, col. 4, lines 55-58) for said accelerator logic and performs page faulting (memory controller 20 manages page faults, col. 5, lines 1-3) of said texture data, invisibly to the host processor (Fig. 1 shows the memory controller 20 coupled between memory 10 and a plurality of memory clients and does not involved host processor and thus is considered invisible to the host processor). Therefore, at least claims 3 and 13 are anticipated by Mizuyabu.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuyabu et al (6,297,832 hereinafter "Mizuyabu") in view of Porterfield (6,249,853).

The teachings of Mizuyabu are given in previous paragraph of this Office action. However, Mizuyabu fails to explicitly suggest or teach said first memory management logic is a bridge controller. This is what Porterfield teaches (Fig. 3, system logic 154 includes a main memory controller to control/manage the access of the main memory 156, col. 6, lines 22-24). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Porterfield into the computer system of Mizuyabu in order to manage or control the access of the main memory in efficient and effective manner. Therefore, at least claim 12 would have been obvious.

8. Claims 4, 5, 7, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peddada et al (6,295,068 hereinafter "Peddada") in view of Emberling et al (6,246,422 hereinafter "Emberling").

As per claim 4, Peddada teaches a computer system (Fig. 5) comprising a host processor (CPU 10) having host physical memory (main memory 12) associated therewith, and a graphics accelerator unit (3D graphics accelerator 20) having respective local memory (memory 22 and 24) associated therewith; wherein, when said graphics accelerator unit attempts to access texture data which is in said physical memory associated with said host, said graphics memory manager fetches said texture data automatically (col. 6, lines 22-39). However, Peddada fails to explicitly teach the graphics accelerator unit also having a graphics memory manager. Peddada teaches a

3D graphics driver (60) to manage the texture data. Emberling teaches a graphics subsystem/accelerator (112) includes a graphics processing core (66), a texture memory (40) may be implemented as part of the main memory (Fig. 10), a RAMDAC (198) and a storage logic (64) manages texture data in the texture memory. Emberling further teaches some of the functionality of storage logic 64 may be replace by CPU 102 and appropriate software (col. 8, lines 46-57). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Emberling into the system of Peddada in order to more efficiently accessing the texture data and thus increase the performance of the graphics system.

As per claim 5, Peddada teaches after fetching said texture data, said graphics memory manager restarts texture processing (col. 5, lines 30-40).

As per claim 7, Peddada teaches a computer system (Fig. 5) comprising a host processor (CPU 10) having host physical memory (main memory 12) associated therewith, and also having virtual memory management (not shown in the figures, but is inherent to any well known computer system to include MMU to manage virtual memory); and a graphics accelerator unit (3D graphics accelerator 20) having respective physical memory (memory 22 and 24) associated therewith, and also having a virtual memory management (see rejection on claim 4 above); and wherein, when said graphics accelerator unit attempts to access texture data which is in said host physical memory, if said texture data is in said host physical memory, said graphics memory manager fetches said texture data therefrom automatically (col. 6, lines 22-39); and if said texture data is not in said host physical memory, said texture data is first

loaded into said host physical memory, and thereafter said graphics memory manager fetches said texture data automatically from said host physical memory (col. 5, lines 61-67 and col. 6, lines 14-39). Therefore, at least claim 7 would have been obvious.

As per claims 16 and 19, Peddada teaches said host processor is operatively connected to receive inputs from input devices (inherently, such as, mouse, keyboard) through an interface manager chip (system logic chipset 16) which provides an interface to various ports and register.

As per claim 18, Peddada teaches means for determining where a page is located in host physical memory (col. 5, lines 57-61); means for updating page tables for said page (col. 5, lines 61-65); means for downloading said page (col. 6, lines 3-13); means for restarting texture processing (col. 6, lines 14-39).

Response to Arguments

9. Applicant's arguments filed 8/19/04 have been fully considered but they are not persuasive.

Regarding claim 11, applicant argues that figure 1 of the drawings shows the claimed feature. The examiner disagrees. Figure 1 shows **a computer system** comprising a CPU, a user input device, a microprocessor and an output device. However, claim 1 requires a **CPU comprising** a user input device, a microprocessor and an output device.

Regarding claims 2 and 8-10, applicant argues that the specification beginning on page 8, line 11, teaches the claimed "a graphics accelerator unit which "***manages***" page faulting of texture data, ***from*** dedicated graphics memory into a main memory ...".

However, the portion of the specification how the graphics accelerator "manages" page faulting of texture data from graphics memory into a main memory" where applicant considered "memory manager" dynamic memory allocation (see page 19 of the remark).

Regarding 35 USC 102(b) of claims 1, 3 and 13, applicant argues that Mizuyabu do not appear to offload the functions of their video graphics system from the main CPU. The examiner disagrees. The 3D and 2D graphics image processors, and other graphics and video display engines ... of Mizuyabu are specific processors which performs the functions normally performed by CPU and are considered offload from the CPU to one of ordinary skill in the art.

Applicant further argues that the memory controller 20 of Mizuyabu manages page faulting and is not invisibly to the host processor. The examiner disagrees because the memory controller of Mizuyabu manages the page faulting and by receiving a memory access request from one of the plurality of clients (30-80) without CPU intervention by includes a scheduler 22 and a sequencer 24 (col. 5, lines 1-8).

Applicant further argues that Mizuyabu does not appear to disclose a graphics accelerator unit and processors 70 and 80 could not be considered to be rendering accelerator logic. The examiner disagrees because Mizuyabu clearly teaches "2D and 3D processors 80 and 70 perform rendering of graphics image" and are part of the video graphics circuit (col. 3, lines 49-53).

Regarding rejection of claims 4, 5, 7, 16, 18 and 19, applicant argues that Peddada does not appear to manage texture memory in the main memory nor does it suggest ***managing page faulting*** of texture data. Well, Peddada clearly teaches

manage texture memory in the main memory (see, figures 4-7). Regarding managing page faulting of texture data, it is noted that the claims 4, 5, 7, 16, 18 and 19 does not appear to require "managing page faulting of texture data".

Regarding prior art to Emberling, applicant argues that storage logic 64 of Emberling is not a memory manager because memory manager by definition are generally to allow dynamic memory allocation. However, the claimed "memory manager" functions to ***fetch texture data***. It is obvious that "fetch texture data" is not equal to "dynamic memory allocation".

Further regarding claim 7, applicant argues that neither of the prior art, discloses or suggests a graphics accelerator unit having virtual memory management and a graphics memory manager. As stated above in the rejection, the teachings of virtual memory management is well known and graphics memory manager is suggest by Emberling. All the arguments have been addressed, and they are not deemed to be persuasive as state above.

Allowable Subject Matter

10. Claims 14, 15, 17 and 20 are allowed.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 703-305-9660. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2676